In the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

1. (Currently Amended) A data processing system comprising:

a memory comprising a plurality of memory locations; and

a central processing unit core comprising at least one register file with a plurality of registers, said core connected to said memory for loading data from and storing data to said memory locations, said core responsive to a load instruction to retrieve ~~at least one data word~~ data words from said memory and parse said ~~at least one data word~~ data words over selected parts of ~~at least~~ two data registers in said at least one register file, ~~wherein the number of said at least two data registers is greater than the number of said at least one data word~~ said parse comprising interleaved unpacking the lower and higher half-words of each of said two data words into corresponding pairs of data registers.

2. (Original) The data processing system of claim 1 wherein said load instruction selects sign or zero extend for the parsed data in said at least two data registers.

3, 4 and 5. (Canceled)

6. (Original) The data processing system of claim ~~5~~ 1 wherein said at least one register file is two register files, and one pair of said corresponding pairs of data registers is located in one register file and the other pair is located in the other register file.

7. (Currently Amended) ~~The~~ A data processing system ~~of claim 1 wherein~~ comprising:

a memory comprising a plurality of memory locations; and

B3 a central processing unit core comprising at least one register file with a plurality of registers, said core connected to said memory for loading data from and storing data to said memory locations, said core responsive to a load instruction to retrieve data words from said memory and parse said data words over selected parts of two data registers in said at least one register file, said parse ~~comprises~~ comprising unpacking the bytes of each at least one data word into the lower and higher half-words of each of a pair of data registers.

8. (Original) The data processing system of claim 7 wherein said at least one data word is two data words, and said parse comprises unpacking eight bytes from said two data words into corresponding pairs of data registers.

9. (Original) The data processing system of claim 8 wherein said unpacking of said bytes of said data words is interleaved.

10. (Original) The data processing system of claim 9 wherein said at least one register file is two register files, and one pair of said corresponding pairs of data registers is located in one register file and the other pair is located in the other register file.

11. (Original) The data processing system of claim 7 wherein said at least one register file is two register files, and said pair of data registers are an even/odd pair in the same data register file.

12. (Original) The data processing system of claim 7 wherein said at least one register file is two register files, one of said pair of data registers is located in one register file and the

other is located in the other register file, and each of said pair of data registers has the same relative register number.

13. (Currently Amended) A data processing system comprising:

a memory comprising a plurality of memory locations; and

a central processing unit core comprising at least one register file with a plurality of registers, said core connected to said memory for loading data from and storing data to said memory locations, said core responsive to a store instruction to concatenate data from selected parts of ~~at least~~ two data registers into ~~at least~~ one data word and save said ~~at least~~ one data word to said memory, ~~wherein the number of said at least two data registers is greater than the number of said at least one data word~~, said concatenate packing the lower bytes of the lower and higher half-words of each of said two data registers into said at least one data word.

14. (Canceled)

15. (Currently Amended) The data processing system of claim ~~14~~ 13 wherein said two data registers are an even/odd register pair.

16 to 19. (Canceled)

20. (Currently Amended) ~~The~~ A data processing system ~~of claim 13 wherein said at least two data registers are four data registers, said at least one data word is two data words, and~~ comprising:

a memory comprising a plurality of memory locations; and

a central processing unit core comprising at least one register file with a plurality of registers, said core connected to said memory for loading data from and storing data to said memory

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locations, said core responsive to a store instruction to concatenate data from selected parts of four data registers into two data words and save said two data words to said memory, said concatenate ~~packs~~ packing the lower bytes of the lower and higher half-words of each of said four data registers into said two data words.

21. (New) A data processing system comprising:

a memory comprising a plurality of memory locations; and

a central processing unit core comprising

a plurality of A functional units,

a plurality of B functional units,

an A register file with a plurality of A registers accessed by corresponding register numbers, each A register capable of serving as a source or destination for any A functional unit,

a B register file with a plurality of B registers accessed by corresponding register numbers, each B register capable of serving as a source or destination for any B functional unit,

a first cross path connected to said A register file and said B functional units permitting any one A register file to be a source for at least one B functional unit,

a second cross path connected to said B register file and said A functional units permitting any one B register file to be a source for at least one A functional unit,

said core connected to said memory for loading data from and storing data to said memory locations, said core responsive to a load instruction to retrieve at least one data word from said memory and parse said at least one data word over selected parts of two data registers including an A

register having a first register access number and a second B register having said first register access number.

22. (New) The data processing system of claim 21, wherein said at least one data word comprises a lower data word and an higher data word, and said parse comprises unpacking said lower data word into said A register and said higher data word into said B data register.

23. (New) The data processing system of claim 21, wherein said at least one data word comprises a single data word, and said parse comprises unpacking first and second bytes of said single data word into corresponding lower and higher half words of said A register and third and fourth bytes of said single data word into corresponding lower and higher half words of said B register.

24. (New) The data processing system of claim 23, wherein said load instruction selects sign or zero extend for the parsed data in said A and B registers.

25. (New) The data processing system of claim 21, wherein said at least one data word comprises a single data word, and said parse comprises unpacking first and third bytes of said single data word into corresponding lower and higher half words of said A register and second and fourth bytes of said single data word into corresponding lower and higher half words of said B register.

26. (New) The data processing system of claim 25, wherein said load instruction selects sign or zero extend for the parsed data in said A and B registers.

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27. (New) The data processing system of claim 21, wherein said at least one data word comprises a single data word, and said parse comprises unpacking a lower half word of said single data word into a lower half word of said A register and an higher half word of said single data word into a lower half word of said B register.

28. (New) The data processing system of claim 25, wherein said load instruction selects sign or zero extend for the parsed data in said A and B registers.

29. (New) A data processing system comprising:

a memory comprising a plurality of memory locations; and

a central processing unit core comprising

a plurality of A functional units,

a plurality of B functional units,

an A register file with a plurality of A registers accessed by corresponding register numbers, each A register capable of serving as a source or destination for any A functional unit,

a B register file with a plurality of B registers accessed by corresponding register numbers, each B register capable of serving as a source or destination for any B functional unit,

a first cross path connected to said A register file and said B functional units permitting any one A register file to be a source for at least one B functional unit,

a second cross path connected to said B register file and said A functional units permitting any one B register file to be a source for at least one A functional unit,

said core connected to said memory for loading data from and storing data to said memory locations, said core

B3 responsive to a store instruction to concatenate data from selected parts of two data registers including an A register having a first register access number and a second B register having said first register access number into at least one data word.

30. (New) The data processing system of claim 29, wherein said at least one data word comprises a lower data word and an higher data word, and said concatenate comprises packing said A register into said lower data word and said B register into said higher data word.

31. (New) The data processing system of claim 21, wherein said at least one data word comprises a single data word, and said concatenate comprises packing first and third bytes said A register into a lower half word of said single data word and first and third bytes of said B register into an higher half word of said single data word.

32. (New) The data processing system of claim 29, wherein said at least one data word comprises a single data word, and said concatenate comprises packing a first byte of said A register into a first byte of said single data word, a third byte of said A register into a third byte of said single data word, a first byte of said B register into a second byte of said single data word and a third byte of said B register into a fourth byte of said single data word.

33. (New) The data processing system of claim 29, wherein said at least one data word comprises a single data word, and said concatenate comprises packing a lower half word of said A register into a lower half word of said single data word and a lower half

word of said B register into an higher half word of said single data word.

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34. (New) A data processing system comprising:

a memory comprising a plurality of memory locations; and

a central processing unit core comprising

a plurality of A functional units,

a plurality of B functional units,

an A register file with a plurality of A registers accessed by corresponding register numbers, each A register capable of serving as a source or destination for any A functional unit,

a B register file with a plurality of B registers accessed by corresponding register numbers, each B register capable of serving as a source or destination for any B functional unit,

a first cross path connected to said A register file and said B functional units permitting any one A register file to be a source for at least one B functional unit,

a second cross path connected to said B register file and said A functional units permitting any one B register file to be a source for at least one A functional unit,

said core connected to said memory for loading data from and storing data to said memory locations, said core responsive to a load instruction to retrieve ~~at~~ two data words from said memory and parse said data words over selected parts of four data registers including a first A register having a first even register access number, a second A register having a second odd register access number one more that said first even register access number, a first B register having said first even register access number, and a second B register having said second odd register access number.

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35. (New) The data processing system of claim 34, wherein said parse comprises unpacking a first byte of a lower data word into a lower byte of said first A register, a second byte of said lower data word into a third byte of said first A register, a third byte of said lower data word into a first byte of said second A register, a fourth byte of said lower data word into a third byte of said second A register, a first byte of an higher data word into a first byte of said first B register, a second byte of said higher data word into a third byte of said first B register, a third byte of said higher data word into a first byte of said second B register and a third byte of said higher data word into a third byte of said second B data register.

36. (New) The data processing system of claim 35, wherein said load instruction selects sign or zero extend for the parsed data in said first and second A registers and said first and second B registers.

37. (New) The data processing system of claim 34, wherein said parse comprises unpacking a first byte of a lower data word into a lower byte of said first A register, a third byte of said lower data word into a third byte of said first A register, a second byte of said lower data word into a first byte of said second A register, a fourth byte of said lower data word into a third byte of said second A register, a first byte of an higher data word into a first byte of said first B register, a third byte of said higher data word into a third byte of said first B register, a second byte of said higher data word into a first byte of said second B register and a third byte of said higher data word into a third byte of said second B data register.

38. (New) The data processing system of claim 37, wherein said load instruction selects sign or zero extend for the parsed data in said first and second A registers and said first and second B registers.

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39. (New) The data processing system of claim 21, wherein said parse comprises unpacking a lower half word of a lower data word into a lower half word of said first A register, a higher half word of said lower data word into a lower half word of said second A register, a lower half word of a higher data word into a lower half word of said first B register and a higher half word of said higher data word into a lower half of said second B register.

40. (New) The data processing system of claim 39, wherein said load instruction selects sign or zero extend for the parsed data in said first and second A registers and said first and second B registers.

41. (New) The data processing system of claim 34, wherein said parse comprises unpacking a lower half word of a lower data word into a lower half word of said first A register, a lower half word of a higher data word into a lower half word of said second A register, a higher half word of said lower data word into a lower half word of said first B register and a higher half word of said higher data word into a lower half of said second B register.

42. (New) The data processing system of claim 41, wherein said load instruction selects sign or zero extend for the parsed data in said first and second A registers and said first and second B registers.

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43. (New) A data processing system comprising:

a memory comprising a plurality of memory locations; and

a central processing unit core comprising

a plurality of A functional units,

a plurality of B functional units,

an A register file with a plurality of A registers accessed by corresponding register numbers, each A register capable of serving as a source or destination for any A functional unit,

a B register file with a plurality of B registers accessed by corresponding register numbers, each B register capable of serving as a source or destination for any B functional unit,

a first cross path connected to said A register file and said B functional units permitting any one A register file to be a source for at least one B functional unit,

a second cross path connected to said B register file and said A functional units permitting any one B register file to be a source for at least one A functional unit,

said core connected to said memory for loading data from and storing data to said memory locations, said core responsive to a store instruction to concatenate data from selected parts of four data registers including a first A register having a first even register access number, a second A register having a second odd register access number one more that said first even register access number, a first B register having said first even register access number, and a second B register having said second odd register access number into two data words.

44. (New) The data processing system of claim 43, wherein said concatenate comprises packing a first byte of said first A

B3 register into a first byte of a lower data word, a third byte of said first A register into a second byte of said lower data word, a first byte of said second A register into a third byte of said lower data word, a third byte of said second A register into a fourth byte of said lower data word, a first byte of said first B register into a first byte of a higher data word, a third byte of said first B register into a second byte of said higher data word, a first byte of said second B register into a third byte of said higher data word and a third byte of said second B register into a fourth byte of said higher data word.

45. (New) The data processing system of claim 43, wherein said concatenate comprises packing a first byte of said first A register into a first byte of a lower data word, a third byte of said first A register into a third byte of said lower data word, a first byte of said second A register into a second byte of said lower data word, a third byte of said second A register into a fourth byte of said lower data word, a first byte of said first B register into a first byte of a higher data word, a third byte of said first B register into a third byte of said higher data word, a first byte of said second B register into a second byte of said higher data word and a third byte of said second B register into a fourth byte of said higher data word.

46. (New) The data processing system of claim 43, wherein said concatenate comprises packing a lower half word of said first A register into a lower half word of a lower data word, a higher half word of said first A register into a higher half word of said lower data word, a lower half word of said first B register into a lower half word of a higher data word and a lower half word of said second B register into a higher half word of said higher data word.

B3 47. (New) The data processing system of claim 43, wherein said concatenate comprises packing a lower half word of said first A register into a lower half word of a lower data word, a higher half word of said first A register into a lower half word of a higher data word, a lower half word of said first B register into a higher half word of said lower data word and a lower half word of said second B register into a higher half word of said higher data word.